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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,135	11/18/2003	William A. Polinsky	MICS:0122 (03-0208)	7023

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,135	POLINSKY ET AL.	
	Examiner	Art Unit	
	Evan Pert	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) ✓

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by US 3,619,249 [see "Example 7" at col. 7].

3. Claims 1-2, 6-8, 10-11, 14-22 and 28-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. (US 2002/0086118 A1).

Regarding claim 1, the '118 document discloses a method for forming polymer within a reaction chamber [0022, last sentence, indicating that the invention "promotes the adhesion of polymer deposited on interior surfaces of the reaction chamber during a plasma etch process"], the process comprising: providing a reaction chamber (152); introducing a polymer-forming gas within the reaction chamber ([0035]-[0037]); and regulating an environment within the chamber to form a polymer on an interior surface of the chamber ([0042]-[0043] in view of prior art [0006], taken with applicant's specification, p. 8, line 18 to p. 9, line 8, detailing what is needed "to form a polymer" as claimed).

Regarding claim 2, the wafer is in the chamber when polymer is deposited on the interior of the chamber (e.g. during a plasma etch, [0040]).

Regarding claim 7, the chamber is an "etch reactor" [0038].

Regarding claim 8, the '118 document discloses a method of manufacturing an integrated circuit [0036], the method comprising the acts of: disposing a semiconductor wafer in a reaction chamber [0036]; processing the semiconductor wafer in the reaction chamber ([0036] + [0005] + [0006]); and providing a polymer-building gas in the reaction chamber to create a layer of polymer on an interior portion of the reaction chamber ([0022] + [0035]).

Regarding claim 10, the polymer-building gas is provided during processing of the semiconductor wafer in the reaction chamber ([0036] to [0037]).

Regarding claims 6 and 11, the polymer-building gas is a "fluorocarbon" such as "trifluoromethane" (CHF_3) or "octofluorocyclobutane" (C_4F_8) ([0035] in view of [0006]).

Regarding claims 14-16, the wafer in the chamber is a layered wafer where at least one layer was formed through deposition, and including an ARC layer, for example [0005].

Regarding claims 17 and 19, the "etching" procedure is a "patterning" of the semiconductor wafer, as is known in the art [0005].

Regarding claim 18, the etching that deposits polymer on interior surfaces of the chamber, also deposits polymer material on the semiconductor wafer (i.e. on the sidewalls of the etched features" per [0006]).

Regarding claims 20-22, etching a photoresist layer is disclosed (line 15 of [0038]), the reactor is a plasma reactor, and the polymer-forming gas is provided while etching the photoresist layer (e.g. [0038] in view of [0035]).

Regarding claims 28-29, a "RAM," for example, is a "processor based system," because a RAM is necessarily based on some kind of "processor," to access and manipulate individual memory locations. At [0036]+[0037] of the '118 document, the incorporation of the IC into an electronic device is implicitly disclosed, with the other limitations addressed under the rejection of claim 8.

Regarding claims 30-32, there is an implicit disclosure that memory made in the invention is ultimately to be assembled as part of a computer, the computer necessarily having at least one peripheral, for conveying information into or out of the computer, and some kind of user interface, such as a display, as is notoriously well known [i.e. implicit disclosure anticipates].

4. Claims 1, 3, 5-9, 11 and 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Richardson et al. (US 6,350,697 B1).

Regarding claim 1, the '697 document discloses a method for forming polymer within a reaction chamber, the process comprising: providing a reaction chamber; introducing a polymer-forming gas within the reaction chamber; and regulating an environment within the reaction chamber to form a polymer on an interior surface of the reaction chamber.

Regarding claim 3, the wafer is not in the chamber [abstract].

Regarding claim 5, the pressure range is between about 0 mT to 200 mT because the '697 document discloses "from about 5 to 80 mT" [col. 2, line 50].

Regarding claim 7, the chamber is an etch chamber [e.g. col. 3].

Regarding claim 8, the '697 document discloses a method of manufacturing an integrated circuit [i.e. a method in which a wafer implicitly disclosed as having electronic devices is processed for manufacturing], the method comprising the acts of: disposing a semiconductor wafer in a reaction chamber [i.e. implicitly, for processing, after "conditioning" that deposits polymer on the interior of the chamber walls]; processing the semiconductor wafer in the reaction chamber (wherein the processing is the implicitly disclosed processing following chamber "conditioning" without the wafer in the chamber); and providing a polymer-building gas in the reaction chamber to create a layer of polymer on an interior portion of the reaction chamber (as part of the "conditioning" occurring before a wafer is placed in the chamber for processing).

Regarding claims 6 and 11, "trifluoromethane" (CHF_3) is disclosed as the polymer-building gas [e.g. col. 3, lines 63-64].

Regarding claim 9, the polymer-building gas is provided prior to disposing the semiconductor wafer in the reaction chamber (as part of the chamber "conditioning").

Regarding claims 14-16, the wafer is a layered semiconductor wafer, at least one layer formed through deposition, including an oxide, an ARC and a photoresist [Fig. 2].

Regarding claim 17, the "etching" is "patterning" as is known in the art.

5. Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Richardson et al. or Chang et al., as applied to claim 8 above, and further in view of Moran, Moran being relied on as a secondary reference showing a universal fact in a 102b rejection.

Chang et al. and Richardson et al. are silent about polymer-building gas "reducing the standard deviation of the critical dimensions of the semiconductor wafer," but Moran explains how a polymer on the interior of a process chamber *inherently* "reduces" the standard deviation of semiconductor wafer critical dimensions [invention in view of prior art problems discussed in col. 1]. See also col. 3 of Richardson et al., where they discuss how CDs drift in the prior art.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Richardson et al. or Chang et al., as applied to claim 1 above, and further in view of Official Notice.

Both Chang et al. and Richardson et al. are silent about temperature of the reaction chamber.

The examiner takes Official Notice that temperature is a parameter related to pressure in a plasma etch reactor (PV=nRT), and that temperature is a parameter adjusted to change deposition and etching rates in a plasma processing chamber. While the primary references are silent about temperature, the reactor models cited as exemplary can be operated in the ranged of 90°C to 250°C.

Furthermore, the courts have held that a change of values of a parameter in the prior art is not patentable unless there is an unexpected result. Applicant merely discloses temperatures that allow polymer to form inside the chamber, which is the same goal as the primary references.

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to utilize a temperature in the range of 90°C to 250°C, motivated to produce polymer on the inside walls of the chamber, or to adjust pressure to a desired range, or to heat parts to prevent deposition on those parts [see MPEP 2144].

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al., as applied to claim 8 (and/or 21) above, and further in view of Lee et al. (US 6,080,680).

While Chang et al. mentions etching a photoresist, this reference is silent about providing the polymer-building gas in a relatively small ratio as compared with a reactant gas, Lee et al. is not.

Lee et al. discuss as prior art that small amounts of highly reactive fluorine-containing gases with an oxygen based plasma etch results in higher etch rates, for example [col. 1]

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to add a small amount of polymer-building gas as compared to the oxygen gas for the oxygen plasma, motivated to achieve higher etch rates, for example.

9. Claims 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. or Richardson et al., as applied to claim 8 above, and further in view of Official Notice.

Chang et al. and Richardson et al. are silent about notoriously well-known steps of manufacturing an electronic device including "packaging the IC", "electrically coupling the IC to a substrate circuit board", the electronic device comprising a memory, such as a DIMM (dual in line memory module).

The examiner takes Official Notice that the limitations of the last two lines of claim 23 and the limitations of claims 24-26 are commonly known as "BEOL" or back-end-of-line processing.

It would have been obvious to one of ordinary skill in the art to apply the processing improvements of Chang et al. or Richardson et al. to prior art BEOL processing, motivated to achieve the benefits of Chang et al. or Richardson et al., yet maintain the notoriously well known benefits of packaging a die cut from a wafer, the die being a memory, the memory mounted on a circuit board with other ICs, such as a processor, wherein the whole device is a computer, for example.

Richardson et al. and Chang et al. are also silent about a "DIMM" in particular, while Chang et al. mentions a number of exemplary memory devices that can be made with their improved processing comprising depositing polymer on chamber walls.

It would have been obvious to one of ordinary skill in the art to apply the improvements of Richardson et al. or Chang et al. to an electronic system including a DIMM, motivated to achieve the benefits of improved etching accuracy, for example, and would be motivated to include a DIMM, because with a DIMM you can install memory one at a time in a 64-bit Pentium processor as opposed installing two SIMMS at a time (MPEP 2144, e.g. Webopedia Computer Dictionary),

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Singh et al. (US 6,776,851) is cited for disclosing a process of introducing a polymer-forming gas into a reaction chamber to form a polymer on interior surfaces of the chamber, and could be used in a 102(e) rejection of pending claims.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ETP
January 5, 2005

EVAN PERT
PRIMARY EXAMINER